iridix IP cores (Display)

Dynamic range correction

Version 6

Introduction

Apical's iridix image processing cores provide high-quality contrast optimisation for a wide range of image capture and display devices.

They address the problem of rendering high-quality video on displays of limited dynamic range, without loss of detail or contrast and without clipping of color gamut.

Apical's proprietary dynamic range control algorithms adaptively apply a different tone correction curve to every pixel in the input video frame. Pixel-by-pixel colour correction is additionally provided for unprecedented control of image quality.

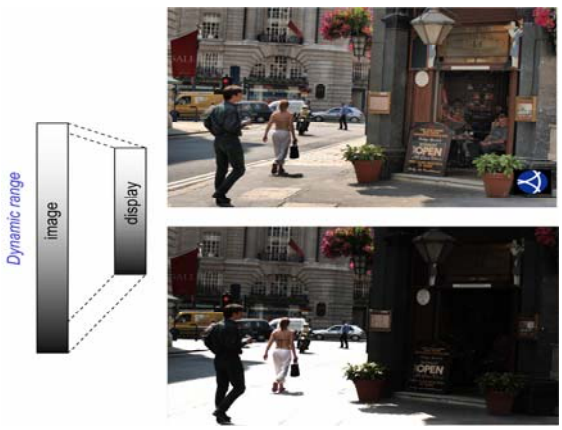
Image content which is normally lost in dark areas can be revealed without damaging bright areas. Regions which are over-saturated can be brought within display range without affecting visibility in dark parts of the image.

For example, when watching a movie on an LCD TV using iridix processing, the viewer gets an experience much closer to that in the movie theatre: all the scene content planned in the original production is visible, the image quality is far more vibrant and dynamic, and colors are preserved perfectly.

Space-variant contrast correction

The *iridix* image processing core analyses the luminance and colour of each pixel in every frame of the input video and generates a space-variant transform which maps every pixel into the display range of a particular device

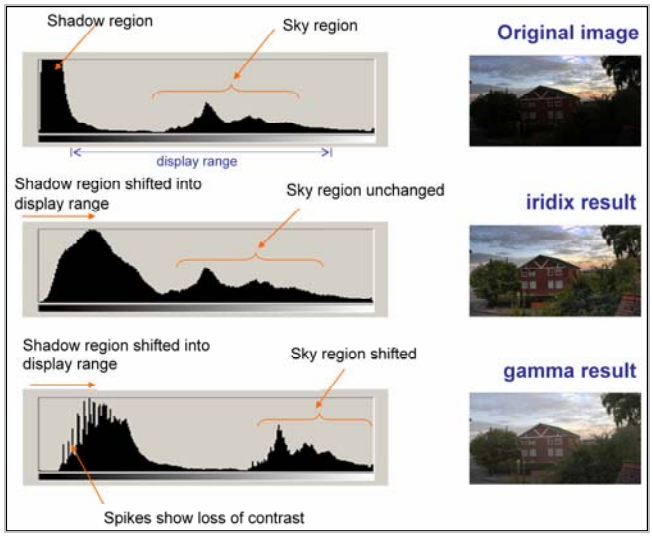
This is achieved without loss of detail, colour or contrast and without generation of artifacts. In addition, deep blacks and pure whites are precisely preserved.



Key features of iridix algorithms

- Adaptive pixel-by-pixel dynamic range correction
- Non-linear colour correction
- Preserves sharpness and fine detail
- Real-time video processing
- Based on human visual perception
- Intuitive but precise parameter controls
- Reveals high-lights and low-lights without affecting well-balanced images
- Automatically generates and applies a different tone curve to every pixel in the input video stream

Comparison with gamma correction



Core overview

All *iridix* DISPLAY cores have been designed for maximum performance at lowest LSI gate count and memory.

They operates synchronously with the video signal and can support up to 1080p at full frame rate and 16 Megapixel still images.

Supported image formats include YUV and RGB at both 8 and 10 bit depths.

The core is fully programmable via a standard two-wire (i^2c compatible) serial interface

Three main versions are available which provide a balance between gate count, memory, performance and cost.

iridix Display core version	Application
High	High-end flat panels
Standard	Middle-range flat panels
Lite	Mobile displays

iridix IP cores (Display)

Dynamic range correction

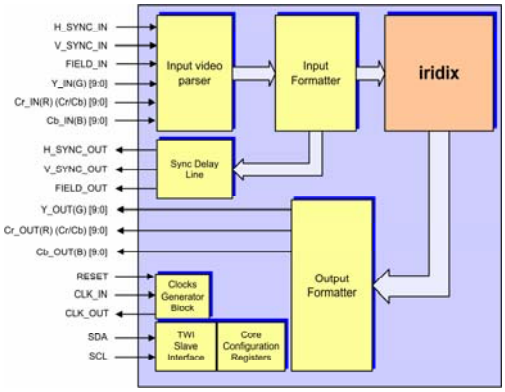
Version 6

Core functional description

The *iridix* core makes a statistical analysis of each input video frame based on the luminance, colour and spatial position of each pixel. This information is held in a multi-dimensional statistics map contained in embedded memory. During the vertical blanking interval, a pixel-by-pixel transform is adaptively generated which adjusts dynamic range while preserving colour, local contrast and fine detail. This transform is applied to each pixel of the following frame of the incoming video stream.

No frame memory is required. Procedures are used which do not require scene change detection. The core can process both progressive and interleaved video in YUV or RGB modes. Internal precision is at least 12 bit, allowing transformation of 8- or 10-bit data without stepping or other artefacts.

Block Schematic



Core features

- Pixel-by-pixel contrast (dynamic range) and colour correction
- Controllable noise suppression
- Still image processing up to 16 Megapixel
- Real-time video up to 1080p
- Compact, low-power core
- No memory interfacing required
- No frame delay
- Core is fully programmable
- Core has been synthesized in silicon

Required clock frequencies

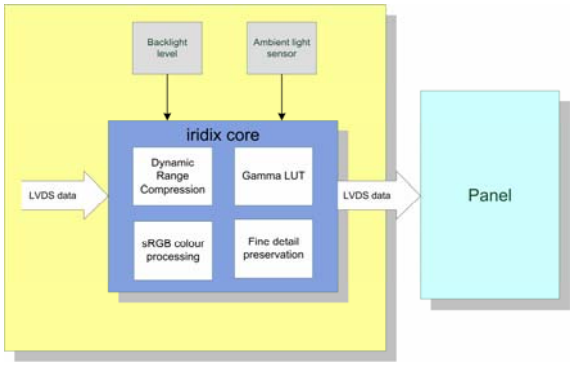
Resolution at 60Hz	480i	720p	1080i 1366x768	1080p	4K digital cinema
Core freq. (MHz)[1]	10	56	63	125	260[3]
Core freq. (MHz)[2]	5	29	32	63	130[3]

1: Highest quality mode. 2: Standard mode. 3: 4K core version.

IP core information

Core	Fully synthesizable HDL source
Principal modules	Spatial & intensity filtering; contrast enhancement; colour correction; fine detail preservation; video interfaces
Digital video formats supported	4:2:2 YUV (8/10-bit interleaved, 16/20-bit non-interleaved) 4:4:4 YCrCb (24/30-bit) 4:4:4 RGB (24/30-bit)
Supported frame sizes	Any from 320x240 to 4096x4096
Video standards	SDTV, HDTV (720p, 768p,1080i,1080p)
LVDS I/O	Yes
Syncronization	Programmable external synchronization mode Internally generated field signal
External memory	Not required
Min. blanking interval	2048 clock cycles
Interrupt	Core processing is fully interruptable and a handshaking protocol is provided
Parameter controls	Two-wire interface serial bus slave, 400kHz (i^2c compatible). Core is fully programmable.

Example implementation



Deliverables

Deliverables comprise: RTL code; Test bench; Behavioural software model; Xilinx FPGA bitstream for real-time evaluation; Software application for register programming; Documentation; Technical support.

For more information, please contact

Apical Limited

Suites 322-324
162-168 Regent Street
London W1B 5TD
United Kingdom

Tel: +44 20 7439 1000
Fax: +44 20 7734 3358

info@apical-imaging.com
www.apical-imaging.com