



# iridix IP cores (DSC)

## Dynamic range correction

### Version 6



## Introduction

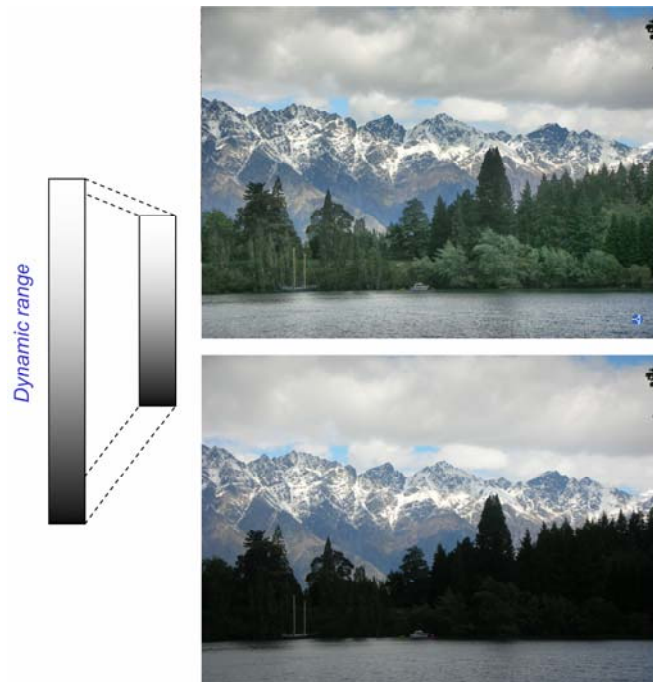
Apical's *iridix* image processing cores provide high-quality contrast optimisation for a wide range of image capture and display devices.

The *iridix* DSC IP cores have been designed specifically for integration into still camera and video pipelines, enabling these devices to produce images which closely match those seen by the human eye.

Apical's proprietary dynamic range control algorithms adaptively apply a different tone correction curve to every pixel in the input video frame. This is coupled with a set of additional proprietary algorithms which control colour and rendering of fine details.

Image content which is normally lost in dark areas can be revealed without damaging bright areas. Regions which are over-saturated can be brought within display range without affecting visibility in dark parts of the image.

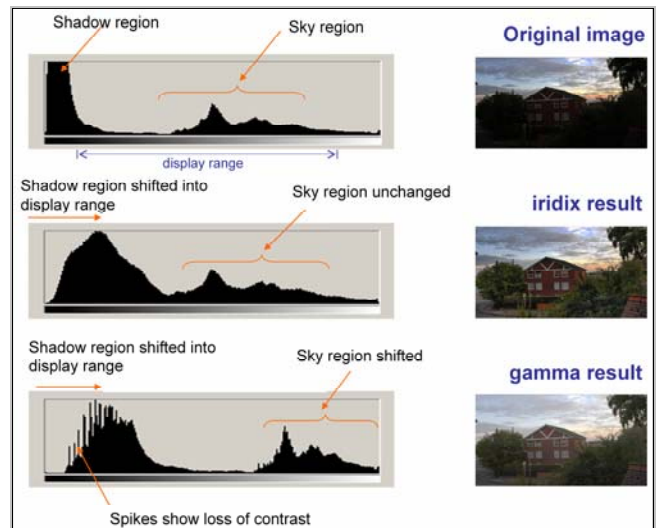
Features enabled by the *iridix* core include dynamic range optimisation, fill flash, Adaptive Digital ISO™, and instant pixel-by-pixel autoexposure.



## Key features of iridix algorithms

- Adaptive pixel-by-pixel dynamic range correction
- Automatically generates and applies a different tone curve to every pixel in the input video stream
- Fast, real-time video processing
- Non-linear colour correction
- Preserves sharpness and fine detail
- Based on human visual perception
- Intuitive but precise parameter controls
- Reveals high-lights and low-lights without affecting well-balanced images

## Comparison with gamma correction



## Core overview

All *iridix* DSC cores have been designed for maximum performance at lowest LSI gate count and memory.

The cores process synchronously at one pixel per clock cycle and require two passes. They are also fully interruptible.

Standard 8 and 10 bit YUV and RGB image formats are supported, together with custom RAW formats up to 16 bits per colour.

The core is fully programmable via a standard two-wire (i<sup>2</sup>c compatible) serial interface

Three main versions are available, depending on whether the core is embedded to process standard 8-bit images or higher dynamic range RAW images. A different core algorithm is used in these three cases.

| iridix DSC core version | Application                                |
|-------------------------|--------------------------------------------|
| High                    | D-SLR (up to 16-bit Bayer + 8 bit formats) |
| Standard                | Compact DSC (8-bit YUV/RGB)                |
| Lite                    | Small core: low gate count and memory      |

## Space-variant contrast correction

The *iridix* image processing core analyses the luminance and colour of each pixel in the original still image or video frame and generates a space-variant transform which maps every pixel into a desired, tunable output range.

This is achieved without loss of detail, colour or contrast and without generation of artifacts. In addition, deep blacks and pure whites are precisely preserved.

The method is based on processing in the human visual system, and always produces natural-looking and high quality images.



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## Core functional description

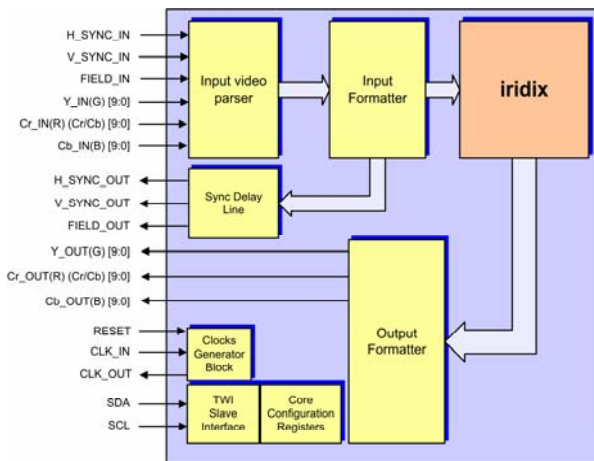
The *iridix* core processing is a two-pass process. During the first pass, the core creates a statistical analysis of each input video frame based on the luminance, colour and spatial position of each pixel. This information is held in a multi-dimensional statistics map contained in embedded memory.

During the second pass, a pixel-by-pixel transform is adaptively generated which adjusts dynamic range while preserving colour, local contrast and fine detail. This transform is applied to each pixel of the following frame of the incoming video stream.

Global parameters, such as strength of processing, together with detailed parameters giving precise control of image quality, can be programmed via a serial bus.

Processing time depends on master clock frequency and image format. Standard implementation requires one clock period per pixel and two passes. Typical processing times are less than 0.1 second for a 10 Megapixel image.

## Block Schematic



## Core features

- Pixel-by-pixel contrast (dynamic range) and colour correction
- Controllable noise suppression
- Still image processing up to 16 Megapixel
- Video processing QVGA, VGA
- Compact, low-power core
- No memory interfacing required
- Core is fully programmable
- Core has been synthesized in silicon

## Deliverables

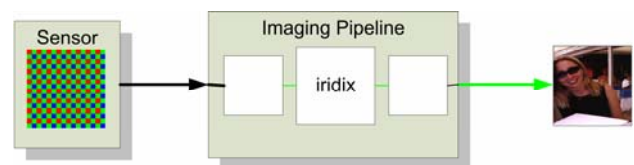
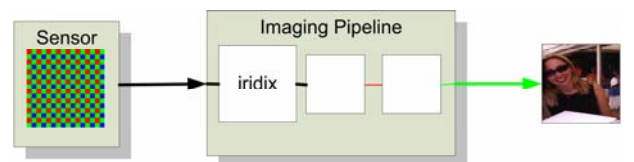
Deliverables comprise: RTL code; Test bench; Behavioural software model; Xilinx FPGA bitstream for real-time evaluation; Software application for register programming; Documentation; Technical support.

## IP core information

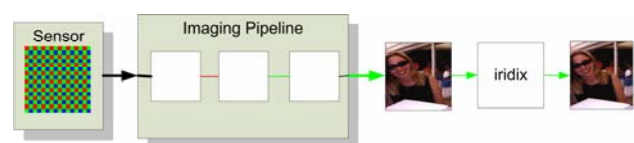
|                                 |                                                                                                                                               |
|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Core                            | Fully synthesizable HDL source                                                                                                                |
| Principal modules               | Spatial & intensity filtering; contrast enhancement; colour correction; fine detail preservation; video/image interfaces                      |
| Digital image formats supported | 4:2:2 YUV (8/10-bit interleaved, 16/20-bit non-interleaved)<br>4:4:4 YCrCb (24/30-bit)<br>4:4:4 RGB (24/30-bit)<br>Camera RAW (Bayer) formats |
| Supported image sizes           | Any from 320x240 to 4096x4096                                                                                                                 |
| Video standards                 | SDTV, HDTV                                                                                                                                    |
| Liveview mode                   | Yes                                                                                                                                           |
| Synchronization                 | Programmable external synchronization mode<br>Internally generated field signal                                                               |
| External memory                 | Not required                                                                                                                                  |
| External CPU                    | Not required                                                                                                                                  |
| Interrupt                       | Core processing is fully interruptible and a handshaking protocol is provided                                                                 |
| Parameter controls              | Two-wire interface serial bus slave, 400kHz (i <sup>2</sup> c compatible). Core is fully programmable.                                        |

## Implementation Options

### In-pipeline processing



### Post-processing



For more information, please contact

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