



iridix IP cores (Video)

Dynamic range correction

Version 6



Introduction

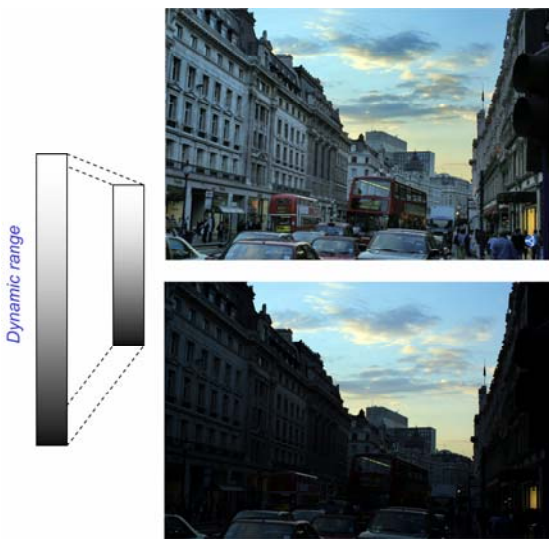
Apical's *iridix* image processing cores provide high-quality contrast optimisation for a wide range of image capture and display devices.

The *iridix* DSC IP cores have been designed specifically for integration into still camera and video pipelines, enabling these devices to produce images which closely match those seen by the human eye.

Apical's proprietary dynamic range control algorithms adaptively apply a different tone correction curve to every pixel in the input video frame. This is coupled with a set of additional proprietary algorithms which control colour and rendering of fine details.

Image content which is normally lost in dark areas can be revealed without damaging bright areas. Regions which are over-saturated can be brought within display range without affecting visibility in dark parts of the image.

In a video camera, *iridix* enables instant, pixel-by-pixel autoexposure which can render the entire range of real-world lighting conditions into standard 8-bit formats without oversaturation, loss of shadow detail or loss of colour and contrast.



Space-variant contrast correction

The *iridix* image processing core analyses the luminance and colour of each pixel in the original still image or video frame and generates a space-variant transform which maps every pixel into a desired, tunable output range.

Typical camera sensors can record a greater range of illumination levels than can be stored or rendered on standard displays. Without efficient dynamic range compression, information is always lost in bright or dark areas. *iridix* is the most effective dynamic range compression engine yet developed and can handle even Wide Dynamic Range scenes up to 16 bits per pixel without loss of any image information

The method is based on processing in the human visual system, and always produces natural-looking and high quality images.

Key features of iridix algorithms

- Adaptive pixel-by-pixel dynamic range correction
- Automatically generates and applies a different tone curve to every pixel in the input video stream
- Fast, real-time video processing
- Non-linear colour correction
- Preserves sharpness and fine detail
- Based on human visual perception
- Intuitive but precise parameter controls
- Reveals high-lights and low-lights without affecting well-balanced images

Video camera screen capture

The frame on the left shows the standard mode of operation, the frame on the right includes *iridix* processing.



Core overview

All *iridix* DSC cores have been designed for maximum performance at lowest LSI gate count and memory. The cores process synchronously at one pixel per clock cycle and require two passes. They are also fully interruptible.

Standard 8 and 10 bit YUV and RGB image formats are supported, together with custom WDR formats up to 16 bits per colour.

The core is fully programmable via a standard two-wire (i²c compatible) serial interface

Two main versions are available, depending on whether the core is embedded to process standard 8-bit images or WDR images. The WDR version can handle source images up to 100dB dynamic range.

iridix video core version	Application
WDR	Security and automotive cameras with double-exposure or other WDR image capture capability
Standard	Consumer and professional video cameras



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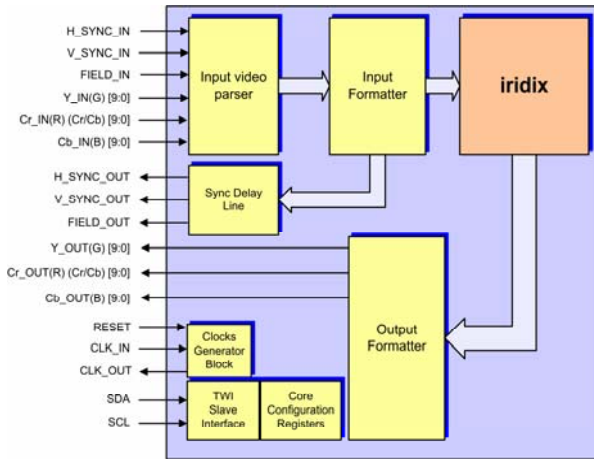


Core functional description

The *iridix* core makes a statistical analysis of each input video frame based on the luminance, colour and spatial position of each pixel. This information is held in a multi-dimensional statistics map contained in embedded memory. During the vertical blanking interval, a pixel-by-pixel transform is adaptively generated which adjusts dynamic range while preserving colour, local contrast and fine detail. This transform is applied to each pixel of the following frame of the incoming video stream.

No frame memory is required. Procedures are used which do not require scene change detection. The core can process both progressive and interleaved video in YUV or RGB modes.

Block Schematic

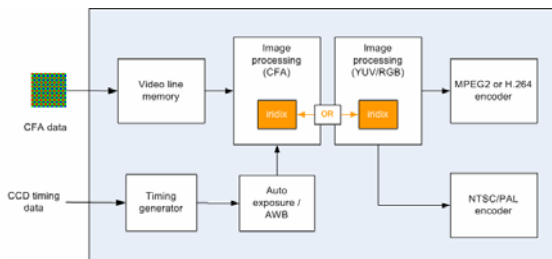


- Compact, low-power core
- No memory interfacing required
- No frame delay
- Core has been synthesized in silicon

Required clock frequencies

Resolution at 60Hz	480i	720p	1080i 1366x768	1080p
Core freq. (MHz) ¹	10	56	63	125
Core freq. (MHz) ²	5	29	32	63

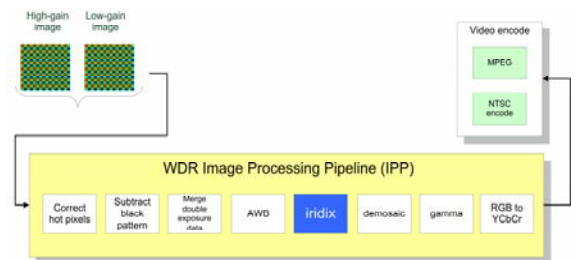
Implementation Example: Video camera



IP core information

Core	Fully synthesizable HDL source
Principal modules	Spatial & intensity filtering; contrast enhancement; colour correction; fine detail preservation; video/image interfaces
Digital image formats supported	4:2:2 YUV (8/10-bit interleaved, 16/20-bit non-interleaved) 4:4:4 YCrCb (24/30-bit) 4:4:4 RGB (24/30-bit) Linear WDR image formats
Supported image sizes	Any from 320x240 to 4096x4096
Video standards	Up to 1080p
Liveview mode	Yes
Synchronization	Programmable external synchronization mode Internally generated field signal
External memory	Not required
External CPU	Not required
Interrupt	Core processing is fully interruptable and a handshaking protocol is provided
Parameter controls	Two-wire interface serial bus slave, 400kHz (i ² c compatible). Core is fully programmable.

Implementation Example: WDR camera



Deliverables

Deliverables comprise: RTL code; Test bench; Behavioural software model; Xilinx FPGA bitstream for real-time evaluation; Software application for register programming; Documentation; Technical support.

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