

## Introduction

Apical provides two complementary Noise Reduction cores on Xilinx FPGA devices.



**Sinter** is a sophisticated but efficient noise reduction module for still images and video. It is an intra-frame processing technology and can be applied inside a DSC pipeline or frame-by-frame to a video source. Based on Apical's proprietary Retina-Morphic processing algorithms, Sinter is able automatically to smooth noisy areas while preserving edges and fine image detail. It is an effective MPEG and JPEG deblocking filter

**Temper** provides high-quality temporal noise reduction for motion video. Frequently video streams contain visible artefacts resulting from sensor or digitisation noise source which is random in time. *Temper* uses sophisticated algorithms to average this noise over successive frames leading to efficient noise reduction without blurring.

The two algorithms work independently. *Temper* is most effective for noise sources which are random in time, such as sensor noise and MPEG2 block artefacts, while *sinter*, provides additional noise reduction for noise which is correlated in time, such as MPEG4 block artefacts.

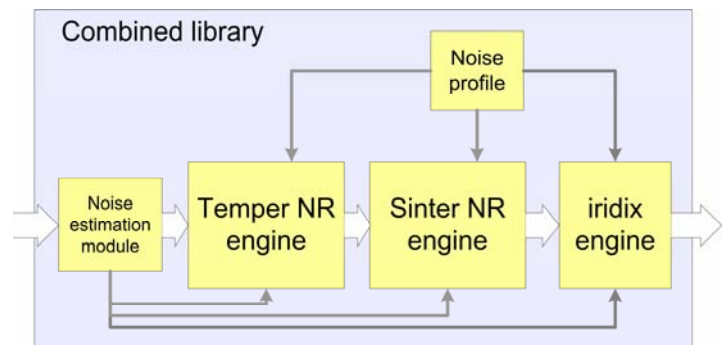
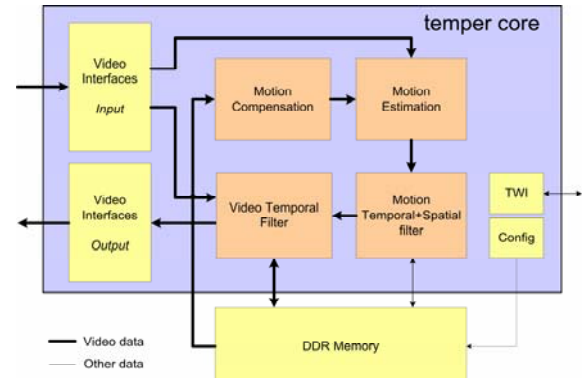


## Main features of temper+sinter cores

- Bayer, YUV or RGB input/ output
- High-quality motion-compensated noise reduction
- High-quality intra-frame noise reduction
- Compression deblocking
- No CPU required
- No frame delay
- Integrated memory controller

## Top-level schematics

*sinter* and *temper* are independent cores and may be used individually or together within an imaging pipeline. They can additionally be used as preprocessing before *iridix* dynamic range compression, enabling stronger enhancement for given source signal-to-noise ratio.



## Core facts

Documentation	User Guide, Design Guide
Design File Formats	EDIF netlist, Verilog, VHDL
Constraints Files	Constraints.ucf
Verification	Test Bench, Test Vectors, Functional using real-time video
Instantiation templates	VHDL, Verilog
Reference designs & application notes	Spartan-3 based layout including mCU, flash memory, analog and digital video interfaces
Additional Items	PC software for parameter control via RS232
Simulation Tool Used	ModelTech's Modelsim
Support	Support provided by Apical Limited



# temper/sinter cores on Spartan3 FPGA

## Noise Reduction

### Version 2

### Example Implementation Statistics

Version	Example Device	Fmax (MHz)	Slices	IOB	GCLK	BRAM	MULT/DSP48	DCM
Standard	XC3S1600E	75	10702	138	5	36	36	3

Versions are also available for other Spartan3 and Virtex 2,4 and 5 devices. Custom implementations can be provided to meet specific interfacing or functional requirements.

### IP core information

Core	Fully synthesizable HDL source
Principal modules	Temporal noise reduction; motion estimation; motion compensation; spatial noise reduction; noise estimation; video/image interfaces
Digital video formats supported	4:2:2 YUV (8/10-bit interleaved, 16/20-bit non-interleaved) 4:4:4 YCrCb (24/30-bit) 4:4:4 RGB (24/30-bit)
Supported frame sizes	Any from 320x240 to 4096x4096
Video standards	SDTV, HDTV (720p, 768p, 1080i)
LVDS I/O	Yes
Synchronization	Programmable external synchronization mode Internally generated field signal
External memory	2 banks 128 MBit DDR/DDR2
Memory controller	Integrated DDR/DDR2 memory controller within netlist/bitstream provided
Line delay	7 lines
Parameter controls	Two-wire interface serial bus slave, 400kHz (i <sup>2</sup> c compatible). Core is fully programmable.

### Core versions

*iridix* IP cores are available in netlist or bitstream form for Xilinx Spartan-3, Spartan-3E, Spartan-3A, Virtex II, Virtex II Pro, Virtex II Pro, Virtex 4 and Virtex 5 devices

For more information, please contact

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